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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/770,478 | 01/29/2001 | James R. Del Signore II | AXI-144 | 6823 |

7590 01/09/2002

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| EXAMINER |
|---|
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | 3 |

DATE MAILED: 01/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/770,478 | DEL SIGNORE II ET AL. | |
| | Examiner | Art Unit | |
| | Quan Tra | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, 9-13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brambilla et al. (USP 5828245) in view of Min et al. (USP 5818212).

As to claims 1, 9 and 16, Brambilla et al. shows in figure 1 a circuit comprising time delay means (21) for eliminating false action; means (18) for providing a voltage ramp, operatively connected to the time delay means; means (load) defining an output voltage; an operational amplifier circuit (16) having a reference input, the operational amplifier circuit receiving the voltage ramp at the reference input; and transistor means (12) electronically connected to the operational amplifier circuit. Thus, figure 1 shows all limitations of the claim except for a capacitor connected to the output node. However, it is well known in the art that capacitor is for filtering. Therefore, it would have been obvious to one having ordinary skill in the art to add a capacitor connected between the output and ground for the purpose of filtering the output signal. Thus, figure 1 shows all limitations of the claim except for the amplifier circuit comparing a divided sample of the output voltage with the voltage ramp. However, Min et al figure 2 shows amplifier circuit 30 comparing a divided output voltage of the output node (Vref2) with a reference voltage for the purpose of having a voltage output higher than the

reference voltage. Therefore, it would have been obvious to one having ordinary skill in the art to have the Brambilla et al.'s amplifier 16 compares the divided output voltage of the output node (Vout) with the voltage ramp for the purpose of having an output voltage higher than the voltage ramp.

As to claim 2, Brambilla et al.'s figure 1 shows all limitations of the claim except for the transistor is a power FET. However, it is well known in the art that power FET is for operating in high power condition. Therefore, it would have been obvious to one having ordinary skill in the art to make transistor 12 as a power transistor for the purpose of operating in a high power condition.

As to claims 3 and 10, it is seen as an obvious design choice for selecting gain value of the amplifier to be two dependeng upon particular environment of use to ensure optimum performance.

As to claims 4 and 11. it is seen as an intended use for selecting the output node to be a point-of-sale printer.

As to claims 5 and 12, it is seen as an obvious design choice for selecting the delay time of the delay means to be approximately 50 ms dependent upon particular environment of use to ensure optimum performance.

As to claims 6 and 13, it is inherent for field effect transistor is operative initially in an OFF state, and subsequently becomes operative in a full-ON state.

3. Claims 7, 8, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brambilla et al. (USP 5828245) in view of Min et al. (USP 5818212) and Maccarrone et al. (USP 5519656).

The combination of Brambilla et al.'s figure 1 and Min et al.'s figure 2 shows all limitations of the claim except for a capacitive means electronically connected to the field effect transistor for ensuring that the field effect transistor is initially operative in the OFF state. However, Maccarrone et al.'s figure 2 shows a capacitor C1 for ensuring transistor (MOUT) is initially in the OFF state and filtering the output of the amplifier. Therefore, it would have been obvious to one having ordinary skill in the art to add a capacitor coupled between the output of the amplifier and ground for the purpose of ensuring the transistor 12 initially in the OFF state and filtering the output of the amplifier.

***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
January 7, 2002

Toan Tran
Primary Examiner